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Complementary metal-oxide-semiconductor (CMOS) technologies are scaled down into the nanometer range, a number of major nonidealities must be addressed and overcome to achieve a successful analog and physical circuit design.

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and current industry projections, we
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Nanotechnology promises to open up new ways of scaling CMOS circuits by introducing new materials. For example, a hybrid circuit of CMOS

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Abstract: Steep subthreshold swing transistors based on interband tunneling are examined toward extending the performance of electronics systems. In particular, this review introduces and summarizes

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progress in the development of the tunnel field-effect transistors (TFETs) including its origin, current experimental and theoretical performance relative to the metal-oxide-semiconductor field ...

Low-Voltage Tunnel Transistors for

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Beyond CMOS Logic ... The leee

ABSTRACT CMOS technology scaling has followed Moore's law well into the nano-scale regime now. The technology scaling is no longer just about geometric reduction but more about innovation in the use of new materials and transistor architectures.

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IEEE, VOL. 87, NO. 4, APRIL 1999

537. Table 1 Technology Scaling
Rules for Three Cases (α Is the
Dimensional Scaling Parameter, β Is the
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nature of these nonidealities has been well reported in the technical literature.

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